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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 0756-2119

First Inventor or Application Identifier: Hisashi OHTANI et al.

Title: SEMICONDUCTOR DEVICE AND PROCESS FOR PRODUCING THE SAME

Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [X] Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original, and a duplicate for fee processing)
2. [X] Specification *Total Pages* [42]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 USC 113) *Total Sheets* [12]
4. [X] Oath or Declaration *Total Pages* [5]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 CFR 1.63(d))
      (for continuation/divisional with Box 17 completed)
      [Note Box 5 below]
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [X] Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

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6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission
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8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement [ ] Power of Attorney
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11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
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17. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
    Divisional of prior application Serial No. 09/197,767, filed November 23, 1998.
    Prior application information: Examiner: P. Cao Group/Art Unit: 2814

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 Docket: 0756-2119

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Application of	)
Hisashi OHTANI et al.	)
Based On Serial No. 09/197,767	) Art Unit: 2814
Which Was Filed: November 23, 1998	) Examiner: P. Cao
For: SEMICONDUCTOR DEVICE AND	)
PROCESS FOR PRODUCING THE	)
SAME	) Date: April 17, 2000

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please preliminarily amend the subject application as follows:

IN THE SPECIFICATION:

Before the first sentence of the specification, insert --This application is a Divisional of Application Serial No. 09/197,767, filed November 23, 1998.--

REMARKS

This application has been amended to include the continuing application data thereof.

Examination on the merits is requested.

Respectfully submitted,

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SEMICONDUCTOR DEVICE AND PROCESS FOR PRODUCING THE SAME

FIELD OF THE INVENTION

The present invention relates to, in a semiconductor device using a thin film, a connection wiring ensuring electric connection between conductive thin films. Particularly, it relates to, in a pixel region of an active matrix liquid crystal display (AMLCD), a connection wiring ensuring electric connection between a switching element and a pixel electrode.

The semiconductor device used herein involves all devices functioning by utilizing semiconductor properties, and an electro-optical device such as an AMLCD and a semiconductor circuit such as a microprocessor are included. Furthermore, an electronic apparatus containing such an electro-optical device and a semiconductor circuit is also included in the semiconductor device.

BACKGROUND OF THE INVENTION

Recently, the technique of providing a TFT on an inexpensive glass substrate is being rapidly developed. This is because the demand of an AMLCD is increased.

In an AMLCD, each of several tens to several millions of pixels arranged in a matrix form is equipped with a thin film transistor (TFT) as a switching element, and input /output of an electric charge on each of pixel electrodes is controlled by the switching function of the TFT.

A liquid crystal is sandwiched between the pixel electrode and a counter electrode to form a kind of capacitor. Therefore, the electro-optical characteristics of the liquid crystal can be changed by controlling input /output of an electric charge on the capacitor, and thus an image can be displayed by controlling light passing through

the liquid crystal panel.

As a characteristic phenomenon in such a display device using a liquid crystal, there is a phenomenon called disclination. While the liquid crystal sandwiched between the pixel electrode and the counter electrode is arranged with orientation having regularity, the orientation may be disturbed by rubbing failure due to unevenness on the surface of the electrodes. The function of light shutter is lost in the location at which disclination occurs, and display failure such as leakage of light arises.

In order to prevent disclination, measures have been conducted such as covering the TFT with a flattened film, but such cannot become drastic countermeasures because flattening of the contact part of the pixel electrode finally produced is impossible even if a flattened film is utilized.

The invention has been developed in view of the above-described problems.

DESCRIPTION OF THE INVENTION

An object of the invention is to provide a technique relating to a constitution of a contact part for forming a completely flat conductive layer.

Particularly, the invention intends to prevent generation of disclination due to a step of a contact part by completely flattening a pixel electrode of an AMLCD, whereby an effective pixel area is enlarged by reducing an area of a black mask, so as to realize an AMLCD of high precision and high contrast.

The invention relates to, as a first aspect, a semiconductor device comprising two conductive layers provided as separate layers, and an insulating layer sandwiched by the two conductive layers,

the two conductive layers being connected to each other with an embedded conductive layer provided as filling an opening formed in the insulating layer, and

the embedded conductive layer comprising an organic resin film containing a conductive material dispersed therein or an inorganic film containing a conductive material dispersed therein.

The invention also relates to, as a second aspect, a semiconductor device comprising two conductive layers provided as separate layers, and an insulating layer sandwiched by the two conductive layers,

the two conductive layers being connected to each other with an oxide conductive layer provided as filling an opening formed in the insulating layer.

The invention further relates to, as a third aspect, a semiconductor device comprising two conductive layers provided as separate layers, and an insulating layer sandwiched by the two conductive layers,

the two conductive layers being connected to each other with an embedded conductive layer provided as filling an opening formed in the insulating layer,

the embedded conductive layer comprising an organic resin film containing a conductive material dispersed therein or an inorganic film containing a conductive material dispersed therein, and

a shape of the opening substantially agreeing with a shape of the embedded conductive layer embedded in the opening.

The invention further relates to, as a fourth aspect, a semiconductor device comprising two conductive layers provided as separate layers, and an insulating layer sandwiched by the two conductive layers,

the two conductive layers being connected to each other with an oxide conductive layer provided as filling an opening formed in the insulating layer, and

a shape of the opening substantially agreeing with a shape of the oxide conductive layer embedded in the opening.

The invention further relates to, as a fifth aspect, a semiconductor device comprising two conductive layers provided as separate layers, and an insulating layer sandwiched by the two conductive layers,

the two conductive layers being connected to each other with an embedded conductive layer provided as filling an opening formed in the insulating layer,

the embedded conductive layer comprising an organic resin film containing a conductive material dispersed therein or an inorganic film containing a conductive material dispersed therein, and

one of the two conductive layers being provided on a flat surface formed by the embedded conductive layer.

The invention further relates to, as a sixth aspect, a semiconductor device comprising two conductive layers provided as separate layers, and an insulating layer sandwiched by the two conductive layers,

the two conductive layers being connected to each other with an oxide conductive layer provided as filling an opening formed in the insulating layer, and

one of the two conductive layers being provided on a flat surface formed by the oxide conductive layer.

The invention further relates to, as a seventh aspect, a process for producing a semiconductor device comprising

a step of forming a first conductive layer,

a step of forming an insulating layer on the first conductive layer,

a step of forming an opening in the insulating layer to expose the first conductive layer at a bottom of the opening,

a step of forming an embedded conductive layer to cover the insulating layer and the opening,

a step of etching or polishing the embedded conductive layer to make a state in that only the opening is filled with the embedded conductive layer, and

a step of forming a second conductive layer on the insulating layer and the embedded conductive layer.

The invention further relates to, as a eighth aspect, a process for producing a semiconductor device comprising

a step of forming a first conductive layer,

a step of forming an insulating layer on the first conductive layer,

a step of forming an opening in the insulating layer to expose the first conductive layer at a bottom of the opening,

a step of forming an oxide conductive layer by a spin coating method to cover the insulating layer and the opening,

a step of etching or polishing the oxide conductive layer to make a state in that only the opening is filled with the oxide conductive layer, and

a step of forming a second conductive layer on the insulating layer and the oxide conductive layer.

The invention further relates to, as a ninth aspect, a process for producing a semiconductor device comprising

a step of forming a first conductive layer,

a step of forming an insulating layer on the first conductive layer,

a step of forming an opening in the insulating layer to

expose the first conductive layer at a bottom of the opening,

a step of forming an embedded conductive layer to cover the insulating layer and the opening,

a step of forming a second conductive layer on the embedded conductive layer,

a step of patterning the second conductive layer to a desired pattern, and

a step of etching the embedded conductive layer by using the second conductive layer as a mask in a self matching manner.

The invention further relates to, as a tenth aspect, a process for producing a semiconductor device comprising

a step of forming a first conductive layer,

a step of forming an insulating layer on the first conductive layer,

a step of forming an opening in the insulating layer to expose the first conductive layer at a bottom of the opening,

a step of forming an oxide conductive layer by a spin coating method to cover the insulating layer and the opening,

a step of forming a second conductive layer on the oxide conductive layer,

a step of patterning the second conductive layer to a desired pattern, and

a step of etching the oxide conductive layer by using the second conductive layer as a mask in a self matching manner.

In the invention, by filling a contact hole with a conductive layer, improvement of the flatness of the second conductive layer (particularly the pixel electrode of the

pixel matrix circuit) formed thereon is intended.

An organic resin film or an inorganic film, in which a material providing conductivity (conductive material) is dispersed, is used as the embedded conductive layer.

Examples of the material for the organic resin film include a polyimide resin, an acrylic resin, a polyamide resin, a polyimideamide resin, an epoxy resin and a polyvinyl alcohol (PVA) resin.

Examples of the inorganic film include a silicon dioxide film of a solution coating type called SOG (spin on glass). Specifically, OCD (Ohka Coating Diffusion source) produced by Tokyo Ohka Kogyo Co., Ltd. and general silicate glass (PSG, BSG and BPSG) can be exemplified.

As the material providing conductivity, a carbon material (such as graphite), zinc oxide, aluminum flakes and nickel flakes can be used. Particularly, graphite is preferred since it is good in general-purpose properties and handling properties. Those having a shape or a particle diameter that cannot fall into the opening provided in the insulating layer cannot be used.

Therefore, the material providing conductivity is preferably in the form of fine particles having a particle diameter of 1/2 or less (more preferably 1/10 or less, particularly preferably 1/100 or less) of the opening width of the opening provided in the insulating layer. For example, in the case where the opening has a diameter of 1 μm (contact hole) to connect the wiring (conductive layers), the material dispersed in the embedded conductive layer preferably has a diameter of 0.5 μm or less (more preferably 0.1 μm or less, particularly preferably 0.01 μm or less).

The inventors have selected a solution coating type conductive layer as a material that is preferred for filling

in the fine contact hole, and have given attention to an ITO (indium tin oxide) film of a solution coating type as a representative material thereof.

Examples of the ITO film include a thin film produced by using ADEKA ITO coating solution produced by Asahi Denka Kogyo K.K. While an indium tin organic compound is dissolved in a xylene solvent to form this ITO coating solution, other oxide conductive layers can be formed by changing the solvent and the solute.

Since the oxide conductive layer is formed as concentrated at the uneven part, it is suitable for effectively filling and flattening the unevenness. The number of coating is not limited to once, and it is effective to coat twice or more to enhance the flatness.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A, 1B and 1C are schematic cross sectional views showing the production process of the connection structure of wiring according to one embodiment of the invention.

Figures 2A, 2B and 2C are schematic cross sectional views showing the production process of the connection structure of wiring in Example 1 according to the invention.

Figures 3A, 3B, 3C and 3D are schematic cross sectional views showing the production process of a pixel matrix circuit in Example 2 according to the invention.

Figures 4A, 4B, 4C and 4D are schematic cross sectional views showing the production process of a pixel matrix circuit in Example 2 according to the invention.

Figures 5A, 5B and 5C are schematic cross sectional views showing the production process of a pixel matrix circuit in Example 2 according to the invention.

Figures 6A, 6B, 6C and 6D are schematic cross sectional

views showing the production process of a pixel matrix circuit in Example 3 according to the invention.

Figures 7A, 7B, 7C and 7D are schematic cross sectional views showing the production process of a pixel matrix circuit in Example 3 according to the invention.

Figures 8A, 8B and 8C are schematic cross sectional views showing the production process of a pixel matrix circuit in Example 3 according to the invention.

Figures 9A, 9B and 9C are schematic cross sectional views showing the production process of a pixel matrix circuit in Example 7 according to the invention.

Figures 10A, 10B and 10C are schematic cross sectional views showing the production process of a pixel matrix circuit in Example 8 according to the invention.

Figures 11A and 11B are schematic perspective views of electro-optical device of Example 11 according to the invention.

Figures 12A to 12F are schematic perspective views of electronic apparatuses of Example 13 according to the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

One embodiment of the invention is described with reference to Figures 1A to 1C. In Figure 1A, numeral 100 denotes an underlayer, which may be any of an insulating layer, a semiconductor layer or a conductive layer, and a first conductive layer 101 having a pattern is formed thereon.

The first conductive layer 101 is covered with an insulating layer (interlayer insulating layer) 102. As the insulating layer 102, an insulating film containing silicon such as silicon oxide, silicon nitride and silicon oxide nitride, or an organic resin layer is used as a single layer

or as having a multilayer structure. The case where an organic resin layer is provided as a single layer is described herein, for example.

After forming the insulating layer 102, an opening (contact hole) 103 is formed by etching. The method for etching may be a wet etching method or a dry etching method. It is effective that the cross sectional shape of the opening 103 is tapered to improve the coverage of a thin film subsequently formed.

After forming the opening 103, an embedded conductive layer 104 is formed. As the embedded conductive layer 104, an organic resin film containing a carbon material dispersed therein or an inorganic resin film containing a carbon material dispersed therein is used. A solution containing the carbon material dispersed therein is coated on the insulating layer 102, and an excess of the solution is removed by spin drying, to form the thin film. This technique is called a spin coating method.

After forming the embedded conductive layer 104 by the spin coating method, an excess of the solvent is removed by a baking (curing) step to improve the film quality depending on necessity. The conditions for the curing step are not limited, and baking (heat treatment) at 300°C for 30 minutes is generally required.

The advantages of the thin film formed by coating a solution are that the film formation is extremely easy, and the film thickness can be easily increased. Furthermore, since the film is in the form of solution in the stage of film forming, it exhibits excellent covering properties of minute unevenness and is extremely suitable for filling a minute opening such as the contact hole. The invention has been attained with making attention to such excellent

covering properties of a material of solution coating type.

Another advantage of the material of solution coating type is easiness of coloring. For example, a black colored organic resin film by dispersing a carbon series material is utilized as a black mask.

The inventor have made attention to the fact that among the organic resin films containing carbon material dispersed therein, an organic resin film using graphite as the carbon material becomes a film having a low resistance, and have found that it is used as the conductive layer for filling a contact hole, with combining the excellent covering properties of the material of solution coating type.

The state of Figure 1A can be obtained after forming the embedded conductive layer 104. After that, the embedded conductive layer 104 is subjected to an etch back process by a dry etching method, to obtain a state in which the embedded conductive layer 104 fills only the opening 103, as shown in Figure 1B.

In the etch back process, the etching selectivity of the insulating layer 102 and the embedded conductive layer should be noted. Since an organic resin film is used as the insulating film 102 in Figure 1A, it is etched to the extent similar to the embedded conductive layer 104 in the etch back process, and no step is formed therebetween.

However, in the case where the insulating layer 102 is a silicon oxide film, the etch back process must be terminated at the time when the silicon oxide film is exposed, otherwise only the embedded conductive layer 104 is etched in the opening to form a step at the opening.

In view of the above, it is preferred that the insulating layer 102 and the embedded conductive layer 104 are in the conditions in that they have the same etching

selectivity as possible. In order to accomplish such conditions, the etching conditions may be optimized or the same material is used in both the insulating layer 102 and the embedded conductive layer 104.

It is an important factor in the invention that the film thickness can be easily increased. In Figure 1A, the thickness of the embedded conductive layer 104 must be the same as or thicker than the thickness of the insulating layer 102. Therefore, a CVD method and a sputtering method are not practical since the throughput is rather deteriorated by using these methods.

After thus obtaining the state shown in Figure 1B, a second conductive layer 105 is formed to have a pattern. As a result, the two conductive layers (the first conductive layer 101 and the second conductive layer 105) insulatedly separated by the insulating layer 102 are electrically connected through the embedded conductive layer 104, as shown in Figure 1C. The second conductive layer 105 can maintain complete flatness even at a contact part 106.

The invention having the above-described constitution is further described in detail with reference to the following examples.

EXAMPLE 1

In this example, ITO is used as the embedded plug (conductive layer). In Figure 2A, numeral 200 denotes an underlayer, which may be any of an insulating layer, a semiconductor layer or a conductive layer, and a first conductive layer 201 having a pattern is formed thereon.

The first conductive layer 201 is covered with an insulating layer (interlayer insulating layer) 202. As the insulating layer 202, an insulating film containing silicon such as silicon oxide, silicon nitride and silicon oxide-

nitride, or an organic resin layer is used as a single layer or as having a multilayer structure.

After forming the insulating layer 202, an opening (contact hole) 203 is formed by etching. The method for etching may be a wet etching method or a dry etching method. It is effective that the cross sectional shape of the opening 203 is tapered to improve the coverage of a thin film subsequently formed.

After forming the opening 203, an oxide conductive layer 204 is formed. As the oxide conductive layer 204, an ITO film of solution coating type is used. A solution containing an indium tin organic compound dissolved in an organic solvent such as xylene is coated on the insulating layer 202, and an excess of the solution is removed by spin drying, to form the thin film. This technique is called a spin coating method.

After forming the oxide conductive layer 204, a drying step at a temperature of from 150 to 170°C and a baking step at 300°C or higher are conducted, and further an annealing step is conducted depending on necessity, to improve the film quality. The conditions of the curing step are not limited to the above, and the optimum conditions may be determined through experiments.

The advantages of the thin film formed by coating a solution are that the film formation is extremely easy, and the covering properties are excellent. That is, since the film is in the form of solution in the stage of film forming, it exhibits excellent covering properties of minute unevenness and is extremely suitable for filling a minute opening such as the contact hole. The invention has been attained with making attention to such excellent covering properties of a material of solution coating type.

In some cases, the ITO film of solution coating type can be colored black by adding a carbon series material or a pigment to the solution for coating the ITO film, and as a result, the light shielding property in the contact hole can be increased.

The state of Figure 2A can be obtained after forming the oxide conductive layer 204. After that, the oxide conductive layer 204 is subjected to an etch back process by a dry etching method, to obtain a state in which the oxide conductive layer 204 fills only the opening 203, as shown in Figure 2B.

In the case where an ITO film is used as the oxide conductive layer, either a wet etching method or a dry etching method may be employed for the etching method in the etch back process.

In the case where the wet etching method is employed, a commercially available etchant for ITO can be used. In the case where the dry etching method is employed, HBr (hydrogen bromide), HI (hydrogen iodide) and CH_4 (methane) can be used as an etching gas. Among these, HBr is preferred from the standpoint of workability and general-purpose properties.

After thus obtaining the state shown in Figure 2B, a second conductive layer 205 is formed to have a pattern. As a result, the two conductive layers (the first conductive layer 201 and the second conductive layer 205) insulatedly separated by the insulating layer 202 are electrically connected through the oxide conductive layer 204, as shown in Figure 2C. The second conductive layer 205 can maintain complete flatness even at a contact part 206.

EXAMPLE 2

In this example, a production process of a unit pixel (unit picture element) constituting a pixel matrix circuit

of an active matrix liquid crystal display device (AMLCD) driven in a reflection mode is described with reference to Figures 3A through 5C.

A quartz substrate 301 having an insulating surface is prepared. In this example, because a heat treatment at a temperature of from 900 to 1,100°C is conducted, a material having high heat resistance must be used. A crystalline glass (glass ceramics) substrate provided with an underlayer film and a silicon substrate provided with a thermal oxidized film may be used.

An amorphous silicon film 302 having a thickness of 65nm is formed thereon, and the amorphous silicon film 302 is crystallized by using the technique described in Unexamined Published Japanese Patent Application No. 8-78329. The technique described in this publication is to conduct selective crystallization by using a catalytic element accelerating crystallization.

A mask insulating film 303 is formed to selectively add a catalytic element (nickel in this example) to the amorphous silicon film 302. An opening 304 is formed in the mask insulating film 303.

A nickel acetate solution containing 10 ppm by weight of nickel is coated by the spin coating method, to form a catalytic element-containing layer 305.

After thus obtaining the state of Figure 3A, removal of hydrogen is conducted at 450°C for 1 hour, and a heat treatment is conducted at 570°C for 14 hours, to obtain a lateral growing region 306. After thus finishing the crystallization step, an addition step of phosphorus is conducted by using the mask insulating film 303 itself as a mask, through which a phosphorus-added region 307 is formed.

After thus obtaining the state of Figure 3B, a heat

treatment at 600°C for 12 hours is conducted, so that nickel remaining in the lateral growing region 306 is subjected to gettering into the phosphorous-added region 307. As a result, a region in which the nickel concentration is lowered to 5×10^{17} atoms/cm^3 (called a gettered region) 308 is obtained as shown in Figure 3C.

Active layers 309 and 310 composed only of the gettered region 308 are formed by patterning, and then a gate insulating film 311 having a thickness of 120 nm is formed. The gate insulating film 311 is composed of a silicon oxide film, a silicon nitride film, a silicon oxide-nitride film, or a laminated film thereof.

After forming the gate insulating film 311, a heat treatment at 950°C for 30 minutes in an oxygen atmosphere is conducted to form a thermal oxidized film at the interface between the active layer and the gate insulating film, by which the interface properties can be largely improved. The active layer 309 and 310 are oxidized to be thinned through the thermal oxidation step. In this example, the thickness of the active layers is finally adjusted to 50 nm. That is, the thickness of the initial film (amorphous silicon film) is 65 nm, and oxidation is conducted for 15 nm, to result in a thermal oxidized film having a thickness of 30 nm. The gate insulating film 311 has a total thickness of 150 nm. The state until this step is shown in Figure 3D.

An aluminum film containing 0.2% by weight of scandium (not shown in figure) is formed, and an island pattern as a base of a gate electrode is formed by patterning. After forming the island pattern, the technique described in Unexamined Published Japanese Patent Application No. 7-135318 is applied, the details of which can be referred to

the publication.

While a resist mask used for patterning remains on the island pattern, anodic oxidation is conducted in a 3% aqueous oxalic acid solution. A formation current of from 2 to 3 mV is applied using a platinum electrode as a cathode to a carry-over voltage of 8V. As a result, porous anodic oxidized films 312 and 313 are formed.

After removing the resist mask, anodic oxidation is conducted in a 3% ethylene glycol solution of tartaric acid neutralized with aqueous ammonia, at which the formation current is from 5 to 6 mV, and the carry-over voltage is 100 V. As a result, dense non-porous anodic oxidized films 314 and 315 are formed.

Gate electrodes 316 and 317 are thus finished through the above-described procedures. In the pixel matrix circuit, gate lines connecting the gate electrodes per one line are formed simultaneously with the formation of the gate electrodes. The state until this step is shown in Figure 4A.

The gate insulating film 311 is etched by using the gate electrodes 316 and 317 and the porous anodic oxidized films 312 and 313 as a mask. The etching is conducted by the dry etching method using CF_3 gas. As a result, the gate insulating films 318 and 319 having the shape shown in Figure 4B are formed.

The porous anodic oxidized films 312 and 313 are removed by the wet etching method. The etching is conducted by using a mixed solution of phosphoric acid, acetic acid and nitric acid, the concentrations of which are 72.3% by weight ±0.1, 9.5% by weight ±1.0 and 2.0% by weight ±0.4, respectively, with water as a solvent.

An impurity ion endowing one conductivity is added by an ion injecting method or a plasma doping method. In the case where the pixel matrix circuit is constituted by an N-type TFT, P (phosphorus) ion is added, and in the case where it is constituted by a P-type TFT, B (boron) ion is added.

The addition of the impurity ion is conducted as separated into two steps. The first step is conducted at a high accelerating voltage of about 80 keV, with the peak of the impurity ion being focused at the lower part of the edge (protruding part) of the gate insulating films 318 and 319. The second step is conducted at a low accelerating voltage of about 5 keV in such a manner that the impurity ion is not added to the lower part of the edge (protruding part) of the gate insulating films 318 and 319.

As a result, source regions 320 and 321, drain regions 322 and 323, low concentration impurity regions (sometimes called an LDD region) 324 and 325, and channel formation regions 326 and 327 are formed, as shown in Figure 4B.

The addition of the impurity ion is preferably conducted so that the sheet resistance of the source/drain region becomes from 300 to 500 Ω per square. The low concentration impurity regions must be optimized according to the performance of the TFT. After completing the addition step of the impurity ion, a heat treatment is conducted to activate the impurity ion.

A silicon oxide film having a thickness of 400 nm is formed as a first interlayer insulating film 328, and contact holes are formed to produce source electrodes 329

and 330 and drain electrodes 331 and 332. In this example, the drain electrodes 331 and 332 are formed as spread within the pixel.

This is a measure of obtaining a capacitance as large as possible, as the drain electrode is used as a lower electrode of an auxiliary capacitance. Because what is produced in this example is a reflection type liquid crystal display device, the lower part of the region at which the pixel electrode is formed later can be freely used without considering the aperture ratio.

After thus obtaining the state shown in Figure 4C, a silicon nitride film 333 having a thickness of 50 nm is formed as covering the source/drain electrodes, and a first metallic film (titanium in this example) 334 is formed thereon. In this example, an auxiliary capacitance is formed between the drain electrode 331 and the first metallic film 334 with using the silicon nitride film 333 as a dielectric material.

An acrylic resin film having a thickness of 1 μm is formed as a second interlayer insulating film 335. Other organic resin films, such as a polyimide resin film, may be used instead of the acrylic resin film. A second metallic film 336 is formed on the second interlayer insulating film 335.

While the second metallic film 336 has a function of a black mask, it mainly functions as an electric field shielding film, i.e., it has a function of protecting the pixel electrode formed later from influence of an electric field generated by the source/drain wiring.

After thus obtaining the state shown in Figure 4D, an acrylic resin film having a thickness of 1 μm is formed as a

third interlayer insulating film 337, and openings 338 and 339 are formed therein. An embedded conductive layer 340 is formed as covering the third interlayer insulating layer 337 and the openings 338 and 339, as shown in Figure 5A.

In this example, an acrylic resin film containing graphite dispersed therein is used as the embedded conductive layer 340. Since the graphite dispersed in the embedded conductive layer 340 is in the form of flakes, it is sufficiently filled in the interior of the openings 338 and 339.

An etch back process is conducted by the dry etching method using an oxygen gas, to realize the state in that the openings 338 and 339 are filled with embedded conductive layers 341 and 342, as shown in Figure 5B.

Pixel electrodes 343 and 344 composed of a material mainly comprising aluminum are formed on the third interlayer insulating film 337 that has been completely flattened by the embedded conductive layers 341 and 342. Because the interior of the contact holes (openings) is filled with the embedded conductive layers 341 and 342, electric connection to the drain electrodes can be realized without forming any step, as shown in Figure 5C.

After that, an alignment film (not shown in figure) is formed on the pixel electrodes 343 and 344 to finish an active matrix substrate, which is one substrate of a liquid crystal display device. The active matrix substrate and a counter substrate prepared according to the conventional manner are fabricated into a cell to finish an active matrix liquid crystal display device.

EXAMPLE 3

In this example, a production process of a unit pixel constituting a pixel matrix circuit of an active matrix

liquid crystal display device (AMLCD) driven in a reflection mode using ITO as an embedded plug (conductive layer) is described with reference to Figures 6A through 8C.

A quartz substrate 601 having an insulating surface is prepared. In this example, because a heat treatment at a temperature of from 900 to 1,100°C is conducted, a material having high heat resistance must be used. A crystalline glass (glass ceramics) substrate provided with an underlayer film and a silicon substrate provided with a thermal oxidized film may be used.

An amorphous silicon film 602 having a thickness of 65nm is formed thereon, and the amorphous silicon film 602 is crystallized by using the technique described in Unexamined Published Japanese Patent Application No. 8-78329. The technique described in this publication is to conduct selective crystallization by using a catalytic element accelerating crystallization.

A mask insulating film 603 is formed to selectively add a catalytic element (nickel in this example) to the amorphous silicon film 602. An opening 604 is formed in the mask insulating film 603.

A nickel acetate solution containing 10 ppm by weight of nickel is coated by the spin coating method, to form a catalytic element-containing layer 605.

After thus obtaining the state of Figure 6A, removal of hydrogen is conducted at 450°C for 1 hour, and a heat treatment is conducted at 570°C for 14 hours, to obtain a lateral growing region 606. After thus finishing the crystallization step, an addition step of phosphorus is conducted by using the mask insulating film 603 itself as a mask, through which a phosphorus-added region 607 is formed.

After thus obtaining the state of Figure 6B, a heat

treatment at 600°C for 12 hours is conducted, so that nickel remaining in the lateral growing region 606 is subjected to gettering into the phosphorus-added region 607. As a result, a region in which the nickel concentration is lowered to 5×10^{17} atoms/cm^3 (called a gettered region) 608 is obtained as shown in Figure 6C.

Active layers 609 and 610 composed only of the gettered region 608 are formed by patterning, and then a gate insulating film 611 having a thickness of 120 nm is formed, as shown in Figure 6D. The gate insulating film 611 is composed of a silicon oxide film, a silicon nitride film, a silicon oxide nitride film, or a laminated film thereof.

After forming the gate insulating film 611, a heat treatment at 950°C for 30 minutes in an oxygen atmosphere is conducted to form a thermal oxidized film at the interface between the active layer and the gate insulating film, by which the interface properties can be largely improved.

The active layer 609 and 610 are oxidized to be thinned through the thermal oxidation step. In this example, the thickness of the active layers is finally adjusted to 50 nm. That is, the thickness of the initial film (amorphous silicon film) is 65 nm, and oxidation is conducted for 15 nm, to result in a thermal oxidized film having a thickness of 30 nm. The gate insulating film 611 has a total thickness of 150 nm. An aluminum film containing 0.2% by weight of scandium (not shown in figure) is formed, and an island pattern as a base of a gate electrode is formed by patterning. After forming the island pattern, the technique described in Unexamined Published Japanese Patent Application No. 7-135318 is applied, the details of which can be referred to the publication.

While a resist mask used for patterning remains on the island pattern, anodic oxidation is conducted in a 3% aqueous oxalic acid solution. A formation current of from 2 to 3 mV is applied using a platinum electrode as a cathode to a carry-over voltage of 8V. As a result, porous anodic oxidized films 612 and 613 are formed.

After removing the resist mask, anodic oxidation is conducted in a 3% ethylene glycol solution of tartaric acid neutralized with aqueous ammonia, at which the formation current is from 5 to 6 mV, and the carry-over voltage is 100 V. As a result, dense non-porous anodic oxidized films 614 and 615 are formed.

Gate electrodes 616 and 617 are thus finished through the above-described procedures. In the pixel matrix circuit, gate lines connecting the gate electrodes per one line are formed simultaneously with the formation of the gate electrodes. The state until this step is shown in Figure 7A.

The gate insulating film 611 is etched by using the gate electrodes 616 and 617 and the porous anodic oxidized films 612 and 613 as a mask. The etching is conducted by the dry etching method using CF_3 gas. As a result, the gate insulating films 618 and 619 having the shape shown in Figure 7B are formed.

The porous anodic oxidized films 612 and 613 are removed by the wet etching method. The etching is conducted by using a mixed solution of phosphoric acid, acetic acid and nitric acid, the concentrations of which are 72.3% by weight ±0.1, 9.5% by weight ±1.0 and 2.0% by weight ±0.4, respectively, with water as a solvent.

An impurity ion endowing one conductivity is added by an

ion injecting method or a plasma doping method. In the case where the pixel matrix circuit is constituted by an N-type TFT, P (phosphorous) ion is added, and in the case where it is constituted by a P-type TFT, B (boron) ion is added.

The addition of the impurity ion is conducted as separated into two steps. The first step is conducted at a high accelerating voltage of about 80 keV, with the peak of the impurity ion being focused at the lower part of the edge (protruding part) of the gate insulating films 618 and 619. The second step is conducted at a low accelerating voltage of about 5 keV in such a manner that the impurity ion is not added to the lower part of the edge (protruding part) of the gate insulating films 618 and 619.

As a result, source regions 620 and 621, drain regions 622 and 623, low concentration impurity regions (sometimes called an LDD region) 624 and 625, and channel formation regions 626 and 627 are formed, as shown in Figure 7B.

The addition of the impurity ion is preferably conducted so that the sheet resistance of the source/drain region becomes from 300 to 500 Ω per square. The low concentration impurity regions must be optimized according to the performance of the TFT. After completing the addition step of the impurity ion, a heat treatment is conducted to activate the impurity ion.

A silicon oxide film having a thickness of 400 nm is formed as a first interlayer insulating film 628, and contact holes are formed to produce source electrodes 629 and 630 and drain electrodes 631 and 632. In this example, the drain electrodes 631 and 632 are formed as spread within the pixel.

This is a measure of obtaining a capacitance as large as

possible, as the drain electrode is used as a lower electrode of an auxiliary capacitance. Because what is produced in this example is a reflection type liquid crystal display device, the lower part of the region at which the pixel electrode is formed later can be freely used without considering the aperture ratio.

After thus obtaining the state shown in Figure 7C, a silicon nitride film 633 having a thickness of 50 nm is formed as covering the source/drain electrodes, and a first metallic film (titanium in this example) 634 is formed thereon. In this example, an auxiliary capacitance is formed between the drain electrode 631 and the first metallic film 634 with using the silicon nitride film 633 as a dielectric material.

A polyimide resin film having a thickness of 1μm is formed as a second interlayer insulating film 635. Other organic resin films, such as an acrylic resin film, may be used instead of the polyimide resin film. A second metallic film 636 is formed on the second interlayer insulating film 635.

While the second metallic film 636 has a function of a black mask, it mainly functions as an electric field shielding film, i.e., it has a function of protecting the pixel electrode formed later from influence of an electric field generated by the source/drain wiring.

After thus obtaining the state shown in Figure 7D, a polyimide resin film having a thickness of 1 μm is formed as a third interlayer insulating film 637, and openings 638 and 639 are formed therein. An oxide conductive layer 640 is formed as covering the third interlayer insulating layer 637 and the openings 638 and 639, as shown in Figure 8A.

In this example, a coating type ITO film having a

viscosity of from 10 to 30 cps (produced by Asahi Denka Kogyo K.K.) is used as the oxide conductive layer 640. After coating the solution by the spin coating method, it is subjected to a drying step at a temperature of from 150 to 200°C for from 5 to 10 minutes and a baking step at a temperature of from 300 to 400°C for from 1 to 2 hours, to improve the film quality. The treatments for improving the film quality is not limited to those conducted in this example.

It is also effective to conduct annealing at a high temperature after the baking step. On conducting annealing, the heat resistance of the material of the electrodes must be considered. In order to avoid the whole of the device subjected to annealing at a high temperature, lamp annealing or the like measure are preferably employed.

The resistance of the oxide conductive layer 640 becomes 1 kΩ per square or less by conducting such a treatment for improving the film quality. It is considered this order of the resistance is enough to ensure electric connection of a submicron distance.

The thickness of the oxide conductive layer 640 can be controlled by the viscosity of the solution, and the rotation number and the rotation speed on spin coating. The thickness must be changed depending on the diameter of the contact holes (opening area), and it is enough to adjust the thickness within the range of from 100 to 500 nm (typically from 150 to 300 nm) to sufficiently fill up the interior of the contact holes.

An etch back process is conducted by the dry etching method using an etching gas selected from HBr, HI and CH_4 diluted with Ar (argon). In this example, HBr is employed. As a result, the state in that the openings 638 and 639 are

filled with oxide conductive layers 641 and 642 is realized, as shown in Figure 8B.

Pixel electrodes 643 and 644 composed of a material mainly comprising aluminum are formed on the third interlayer insulating film 637 that has been completely flattened by the oxide conductive layers 641 and 642. Because the interior of the contact holes (openings) is filled with the oxide conductive layers 641 and 642, electric connection to the drain electrodes can be realized without forming any step, as shown in Figure 8C.

After that, an alignment film (not shown in figure) is formed on the pixel electrodes 643 and 644 to finish an active matrix substrate, which is one substrate of a liquid crystal display device. The active matrix substrate and a counter substrate prepared according to the conventional manner are fabricated into a cell to finish an active matrix liquid crystal display device.

EXAMPLE 4

While the etch back treatment is applied to the embedded conductive electrode or the oxide conductive electrode in Examples 1 to 3, a polishing treatment can be employed instead of the etch back treatment. A technique called CMP (chemical mechanical polishing) can be typically employed.

In the case where this technique is employed, dusts generated during the treatment should be carefully managed. By using this technique, excellent flatness can be ensured even when the third interlayer insulating film and the embedded conductive layer are formed of different materials.

EXAMPLE 5

In Example 2, an acrylic resin layer is employed as the third interlayer insulating film 337, and the main component of the embedded conductive layer is an acrylic resin. Other

organic resins, such as a polyimide resin, may be used as the main component of the embedded conductive layer.

In the case where a silicon oxide film is used as the third interlayer insulating film, it is effective to use a silicon oxide film of solution coating type called SOG as the main component of the embedded conductive layer. In this case, a carbon material, such as graphite, is dispersed in the solution, and the film formation can be conducted by the spin coating method.

The third interlayer insulating film and the embedded conductive layer may be formed of different materials. In such a case, measures should be taken not to form a step at the opening after the etch back treatment.

EXAMPLE 6

While an polyimide film is used as the second and third interlayer insulating films in Example 3, it is effective to use a silicon oxide film or a silicon oxide-nitride film therefor.

Since an organic resin film, such as the polyimide film, only has low heat resistance, the baking temperature of the oxide conductive layer and the subsequent annealing temperature are limited. However, by constituting the interlayer insulating film with a silicon oxide film, etc., annealing at a higher temperature can be realized to obtain a film having further improved film quality.

Since a material mainly composed of aluminum is used as the gate electrode and the source/drain electrode in Example 3, the heat resistance of that material should be considered. However, when a material having high heat resistance is used as the material for the electrodes, an annealing treatment at a high temperature exceeding 500°C can be conducted.

Examples of the material having high heat resistance that can be used as the material for the electrodes in Example 3 include tantalum, tungsten, molybdenum and a silicon film endowed with conductivity.

Furthermore, the constitution in this example and that of Example 4 may be combined.

EXAMPLE 7

In this example, a technique for producing a reflection type AMLCD having a constitution different from Example 2 is described with reference to Figures 9A through 9C.

The state shown in Figure 9A is obtained according to the procedures of Example 2. In Figure 9A, numeral 337 denotes the third interlayer insulating film, and 340 denotes the embedded conductive layer.

Pixel electrodes 901 and 902 composed of a material mainly comprising aluminum are formed on the embedded conductive layer 340. The pixel electrodes 901 and 902 are physically insulated from each other by openings 903 and 904, as shown in Figure 9B.

The embedded conductive layer 340 is etched by using the pixel electrodes 901 and 902 as a mask, to form embedded conductive layers 905 and 906 patterned into the same shape as the pixel electrodes. The embedded conductive layers 905 and 906 are also physically insulated from each other and thus function as a part of the pixel electrodes, as shown in Figure 9C.

According to the constitution of this example, while the openings (corresponding to 903 and 904) separating the pixel electrodes 901 and 902 have a depth of 1 μm or more, this does not bring about any problem since this part positions above the source electrode (source wiring) and is shielded from light. Furthermore, disclination is concentrated at

this part, and thus an effect of preventing disclination spreading to the necessary region in the pixel (pinning effect) can also be expected.

EXAMPLE 8

In this example, a technique for producing a reflection type AMLCD having a constitution different from Example 3 is described with reference to Figures 10A through 10C.

The state shown in Figure 10A is obtained according to the procedures of Example 3. In Figure 10A, numeral 637 denotes the third interlayer insulating film, and 640 denotes the oxide conductive layer.

Pixel electrodes 1001 and 1002 composed of a material mainly comprising aluminum are formed on the oxide conductive layer 640. The pixel electrodes 1001 and 1002 are physically insulated from each other by openings 1003 and 1004, as shown in Figure 10B.

The oxide conductive layer 640 is etched by using the pixel electrodes 1001 and 1002 as a mask, to form oxide conductive layers 1005 and 1006 patterned into the same shape as the pixel electrodes. The oxide conductive layers 1005 and 1006 are also physically insulated from each other and thus function as a part of the pixel electrodes, as shown in Figure 10C.

According to the constitution of this example, while the openings (corresponding to 1003 and 1004) separating the pixel electrodes 1001 and 1002 have a depth of 1 μm or more, this does not bring about any problem since this part positions above the source electrode (source wiring) and is shielded from light. Furthermore, disclination is concentrated at this part, and thus an effect of preventing disclination spreading to the necessary region in the pixel (pinning effect) can also be expected.

Furthermore, the constitution in this example and that of Example 6 may be combined.

EXAMPLE 9

While a TFT having a top gate structure (a planer type herein) is exemplified in Examples 1 to 8, the invention can be easily applied to a TFT having a bottom gate structure (typically a reverse stagger type).

The invention can be applied to not only a TFT but also connection wiring of a MOSFET formed on a single crystal silicon wafer.

As described in the foregoing, the invention can be applied to a device having any structure that requires to connect plural pieces of wiring formed on different layers.

EXAMPLE 10

While an AMLCD driven in a reflection mode is exemplified in Examples 1 to 9, the invention can be applied to an AMLCD driven in a transmission mode. In this case, the constitutions shown in Examples 7 and 8 cannot be applied since the whole of the pixel is shielded from light, but the constitutions shown in Examples 2 and 3 (constitutions in which the embedded conductive layer is filled only in the opening) can sufficiently applied.

In order to produce a transmission type AMLCD, a transparent conductive film (typically an ITO film and a tin oxide film) is used as the pixel electrode.

In the case where a transmission type LCD is produced, when the pixel electrode (transparent conductive film) and the active layer is directly connected to each other, there arises a problem of leakage of light from the contact part. Even in such a case, the opening is filled with the embedded conductive layer to shield the opening from light, and thus the leakage of light can be prevented.

EXAMPLE 11

In this example, an AMLCD fabricated by using the active matrix substrate (substrate on which elements are formed) having the constitution shown in Examples 1 to 10 are exemplified. The appearance of the AMLCD of this example is shown in Figures 11A and 11B.

In Figure 11A, numeral 1101 denotes an active matrix substrate, on which a pixel matrix circuit 1102, a driver circuit on source side 1103 and a driver circuit on gate side 1104 are formed thereon. The driver circuits preferably comprise a CMOS circuit complementarily combining an N-type TFT and a P-type TFT. Numeral 1105 denotes a counter substrate.

In the AMLCD shown in Figure 11A, the active matrix substrate 1101 and the counter substrate 1105 are joined in such a manner that the edges thereof are arranged, provided that a part of the counter electrode 1105 is removed to expose the active matrix substrate 1101, and an FPC (flexible printed circuit) 1106 is connected thereto. Signals from outside are transferred to the inner circuit by the FPC 1106.

IC chips 1107 and 1108 are mounted utilizing the surface on which the FPC 1106 is attached. These IC chips are constituted by forming various circuit, such as a video signal processing circuit, a timing pulse generating circuit, a gamma compensation circuit, a memory circuit and an operation circuit, on a silicon substrate. While two IC chips are mounted in Figure 11A, one IC chip or three or more of them may be mounted.

An AMLCD may have the constitution shown in Figure 11B. In Figure 11B, the same parts as in Figure 11A are denoted by the same symbols, respectively. In this constitution,

the signal processing that is carried out by the IC chips in Figure 11A is conducted by a logic circuit 1109 composed of TFT formed on the same substrate 1101. In this case, the logic circuit 1109 is formed based on a CMOS circuit as similar to the driver circuits 1103 and 1104.

While the AMLCD of this example employs a structure in that the black mask is provided on the active matrix substrate (BM on TFT), the structure in that the black mask may be provided on the counter substrate may be employed.

Display in color may be carried out by using a color filter, or by driving the liquid crystal in an ECB (electric field-controlled birefringence) mode or a GH (guest-host) mode without using a color filter.

Furthermore, a constitution using a microlens array as described in Unexamined Published Japanese Patent Application No. 8-15686 may be employed.

EXAMPLE 12

The constitution of the invention may be applied various electro-optical apparatuses and semiconductor circuits in addition to an AMLCD.

Examples of electro-optical apparatuses other than an AMLCD include an EL (electroluminescence) display apparatus and an image sensor.

Examples of semiconductor circuits include an arithmetic processing circuit such as a microprocessor composed of IC chips and a high frequency module handling an input/output signal of a portable apparatus (such as MMIC).

As described in the foregoing, the invention can be applied to any semiconductor apparatus requiring multilayer wiring technique.

EXAMPLE 13

The AMLCD shown in Example 11 can be utilized as a

display of various electronic apparatuses. The electronic apparatuses exemplified in this example are defined as a product equipped with an active matrix liquid crystal display device.

Examples of such an electronic apparatus include a camcorder, a still camera, a projection display, a projection television, a head-mounted display, a car navigation system, a personal computer (including a notebook computer) and a portable information terminal (such as a portable computer and a cellular phone). Specific examples thereof are shown in Figures 12A through 12F.

Figure 12A shows a cellular phone, which is composed of a main body 2001, a sound output part 2002, a sound input part 2003, a display device 2004, an operation switch 2005 and an antenna 2006. The invention can be applied to the display device 2004.

Figure 12B shows a camcorder, which is composed of a main body 2101, a display device 2102, a sound input part 2103, an operation switch 2104, a battery 2105 and an image receiving part 2106. The invention can be applied to the display device 2102.

Figure 12C shows a portable computer, which is composed of a main body 2201, a camera part 2202, an image receiving part 2203, an operation switch 2204 and a display device 2205. The invention can be applied to the display device 2205.

Figure 12D shows a head mounting display, which is composed of a main body 2301, a display device 2302 and a belt part 2303. The invention can be applied to the display device 2302.

Figure 12E shows a rear type projector, which is composed of a main body 2401, a light source 2402, a display

device 2403, a polarized beam splitter 2404, reflectors 2405 and 2406, and a screen 2406. The invention can be applied to the display device 2403.

Figure 12F shows a front type projector, which is composed of a main body 2501, a light source 2502, a display device 2503, an optical system 2504 and a screen 2505. The invention can be applied to the display device 2503.

As described in the foregoing, the field to which the invention can be applied is extremely broad, and the invention can be applied any electronic apparatus of any field. Furthermore, the invention can be applied to an electric display board and an advertisement display.

The invention relates to a technique for realizing a completely flat pixel electrode in each of pixels constituting a pixel matrix circuit of an AMLCD. The constitution of the invention is particularly effective in a reflection type AMLCD in which the whole surface of the pixel electrode becomes an effective display area.

The disclination generating on the pixel electrode can be effectively prevented, and the effective display area is widely enlarged by practicing the invention. Therefore, high contrast can be realized even in an LCD device of higher precision.

WHAT IS CLAIMED IS:

1. A method for producing a semiconductor device comprising:

a step of forming a first conductive layer;

a step of forming an insulating layer over said first conductive layer;

a step of forming an opening in said insulating layer to expose said first conductive layer at a bottom of said opening;

a step of forming an embedded conductive layer to cover said insulating layer and said opening;

a step of etching or polishing said embedded conductive layer to make a state in that only said opening is filled with said embedded conductive layer; and

a step of forming a second conductive layer on said insulating layer and said embedded conductive layer.

2. A method for producing a semiconductor device comprising:

a step of forming a first conductive layer;

a step of forming an insulating layer over said first conductive layer;

a step of forming an opening in said insulating layer to expose said first conductive layer at a bottom of said opening;

a step of forming an oxide conductive layer by a spin coating method to cover said insulating layer and said opening;

a step of etching or polishing said oxide conductive layer to make a state in that only said opening is filled with said oxide conductive layer; and

a step of forming a second conductive layer on said insulating layer and said oxide conductive layer.

3. A method for producing a semiconductor device comprising:

a step of forming a first conductive layer;

a step of forming an insulating layer over said first conductive layer;

a step of forming an opening in said insulating layer to expose said first conductive layer at a bottom of said opening;

a step of forming an embedded conductive layer to cover said insulating layer and said opening;

a step of forming a second conductive layer on said embedded conductive layer;

a step of patterning said second conductive layer to a desired pattern; and

a step of etching said embedded conductive layer by using said second conductive layer as a mask in a self alignment manner.

4. A method for producing a semiconductor device comprising:

a step of forming a first conductive layer;

a step of forming an insulating layer over said first conductive layer;

a step of forming an opening in said insulating layer to expose said first conductive layer at a bottom of said opening;

a step of forming an oxide conductive layer by a spin coating method, to cover said insulating layer and said opening;

a step of forming a second conductive layer on said oxide conductive layer:

a step of patterning said second conductive layer to a desired pattern, and

a step of etching said oxide conductive layer by using said second conductive layer as a mask in a self alignment manner.

5. A method for producing a semiconductor device according to claim 1, wherein said embedded conductive layer comprises an organic resin film containing a conductive material dispersed therein or an inorganic film containing a conductive material dispersed therein.

6. A method for producing a semiconductor device according to claim 3, wherein said embedded conductive layer comprises an organic resin film containing a conductive material dispersed therein or an inorganic film containing a conductive material dispersed therein.

7. A method for producing a semiconductor device according to claim 5, wherein said conductive material is a carbon material.

8. A method for producing a semiconductor device according to claim 6, wherein said conductive material is a carbon material.

9. A method for producing a semiconductor device according to claim 5, wherein said conductive material is selected from the group consisting of zinc oxide, aluminum flakes and nickel flakes.

10. A method for producing a semiconductor device according to claim 6, wherein said conductive material is selected from the group consisting of zinc oxide, aluminum flakes and nickel flakes.

11. A method for producing a semiconductor device according to claim 2, wherein said oxide conductive layer comprises indium tin oxide.

12. A method for producing a semiconductor device according to claim 4, wherein said oxide conductive layer comprises indium tin oxide.

13. A semiconductor device according to claim 1, 2, 3, 4, 5 or 6 is applied to an EL display device.

14. A method for producing a semiconductor device comprising:
a step of forming a first conductive layer;

a step of forming an insulating layer over said first conductive layer;

a step of forming an opening in said insulating layer to expose said first conductive layer at a bottom of said opening;

a step of forming a second conductive layer to cover said insulating layer and said opening;

a step of polishing said second conductive layer by employing a chemical mechanical polishing; and

a step of forming a third conductive layer on said insulating layer and said second conductive layer.

15. A method for producing a semiconductor device comprising:

a step of forming a first conductive layer;

a step of forming an insulating layer over said first conductive layer;

a step of forming an opening in said insulating layer to expose said first conductive layer at a bottom of said opening;

a step of forming an oxide conductive layer to cover said insulating layer and said opening;

a step of polishing said oxide conductive layer by employing a chemical mechanical polishing; and

a step of forming a second conductive layer on said insulating layer and said oxide conductive layer.

16. A method for producing a semiconductor device according to claim 14, wherein said second conductive layer comprises an organic resin film containing a conductive material dispersed therein or an inorganic film.

17. A method for producing a semiconductor device according to claim 16, wherein said conductive material is a carbon material.

18. A method for producing a semiconductor device according to claim 14, wherein said conductive material is selected from the group consisting of zinc oxide, aluminum flakes and nickel flakes.

19. A method for producing a semiconductor device according to claim 13, wherein said oxide conductive layer comprises Midium tin oxide.

20. A method for producing a semiconductor device according to claim 1, 2, 3, 4, 14 and 15, wherein said semiconductor device is applied to a display device of a cellular phone.

21. A method for producing a semiconductor device according to claim 1, 2, 3, 4, 14 and 15, wherein said semiconductor device is applied to a display device of a camcorder.

22. A method for producing a semiconductor device according to claim 1, 2, 3, 4, 14 and 15, wherein said semiconductor device is applied to a display device of a portable computer.

23. A method for producing a semiconductor device according to claim 1, 2, 3, 4, 14 and 15, wherein said semiconductor device is applied to a display device of a head mounting display.

24. A method for producing a semiconductor device according to claim 1, 2, 3, 4, 14 and 15, wherein said semiconductor device is applied to a display device of a rear type projector.

25. A method for producing a semiconductor device according to claim 1, 2, 3, 4, 14 and 15, wherein said semiconductor device is applied to a display device of a front type projector.

26. A method for producing a semiconductor device according to claim 1, 2, 3, 4, 14 and 15, wherein said semiconductor device is applied to an EL display device.

ABSTRACT OF THE DISCLOSURE

A semiconductor device and a process for producing the same, the semiconductor device comprising two conductive layers provided as separate layers, and an insulating layer sandwiched by the two conductive layers, in which the two conductive layers are electrically connected to each other with an embedded conductive layer or an oxide conductive layer provided as filling an opening formed in the insulating layer, and the embedded conductive layer comprises an organic resin film containing a conductive material dispersed therein or an inorganic film containing a conductive material dispersed therein.

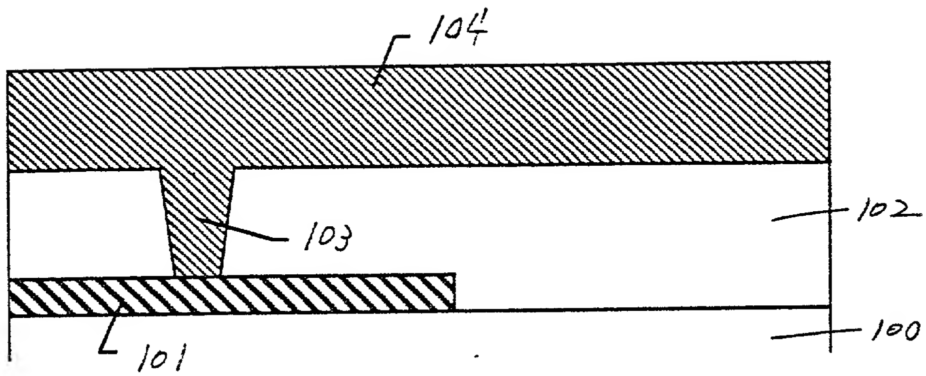

FIG. 1A

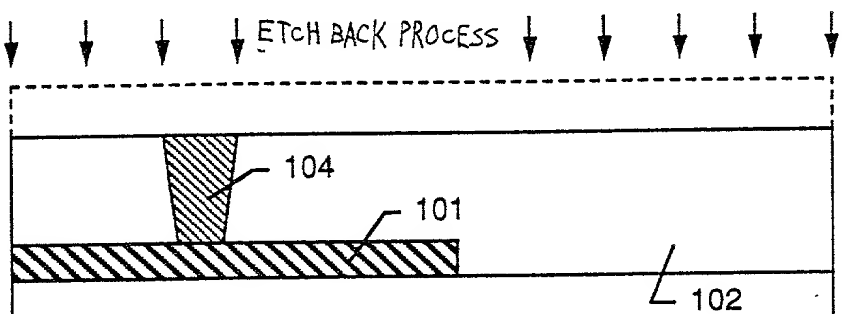

FIG. 1B

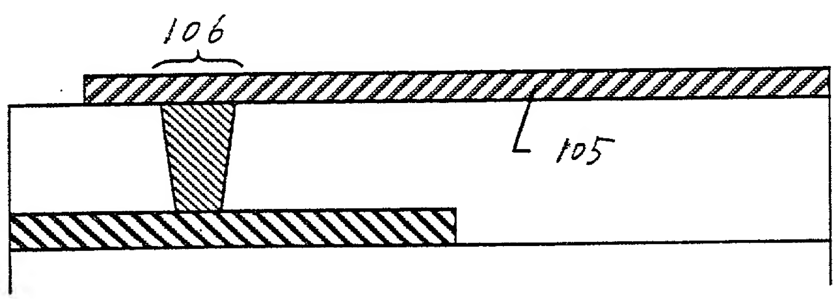

FIG. 1C

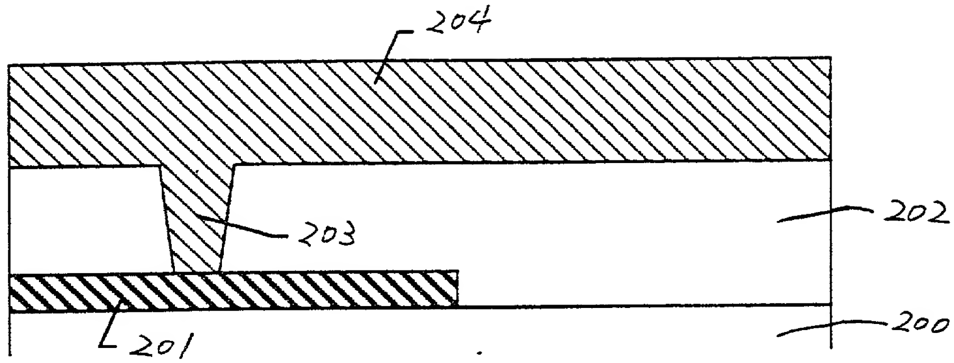

FIG. 2A

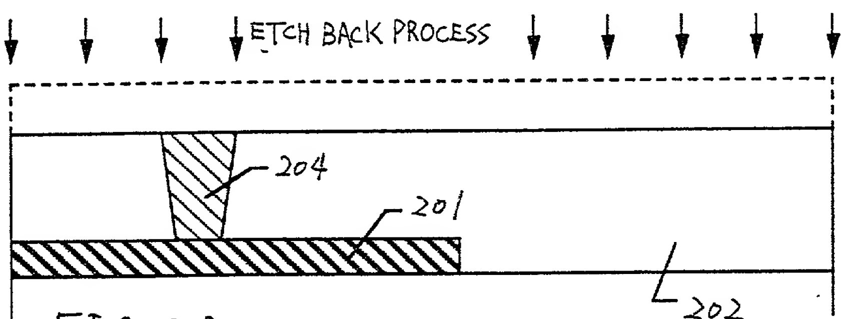

FIG. 2B

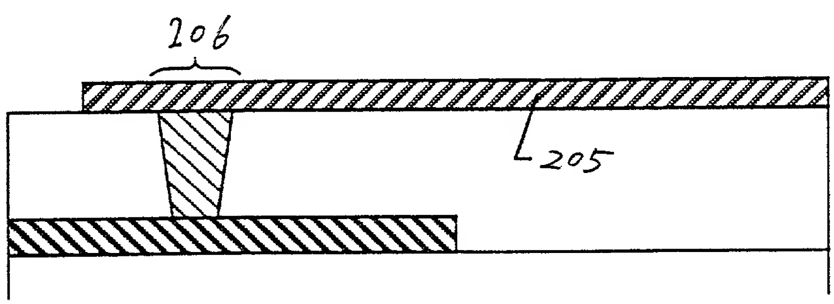

FIG. 2C

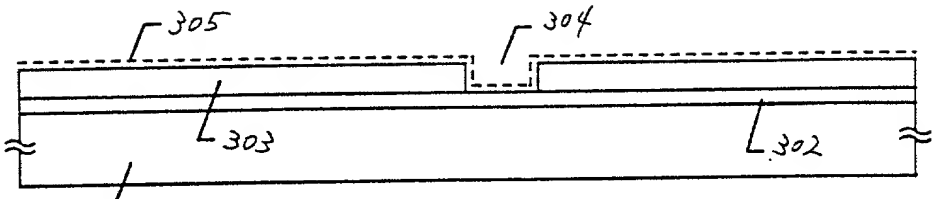

FIG. 3A

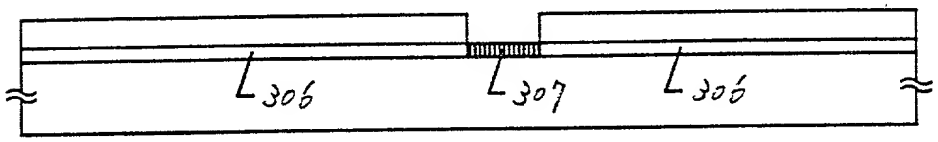

FIG. 3B

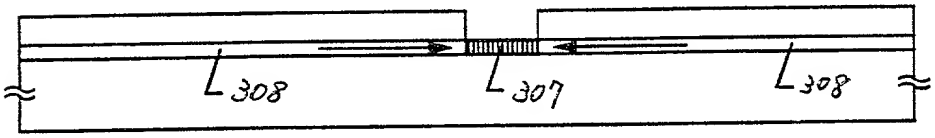

FIG. 3C

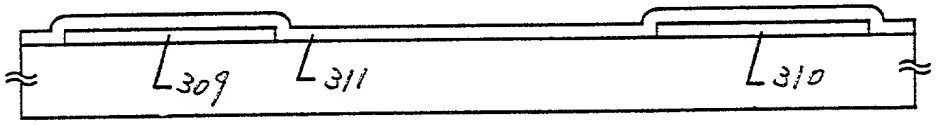

FIG. 3D

FIG. 4A

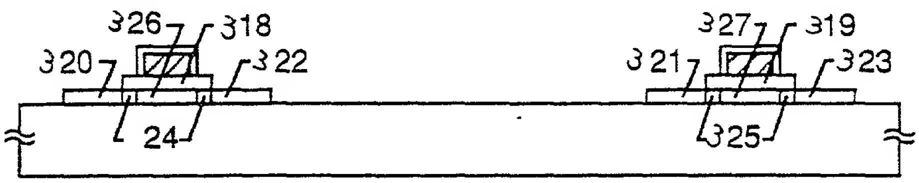

FIG. 4B

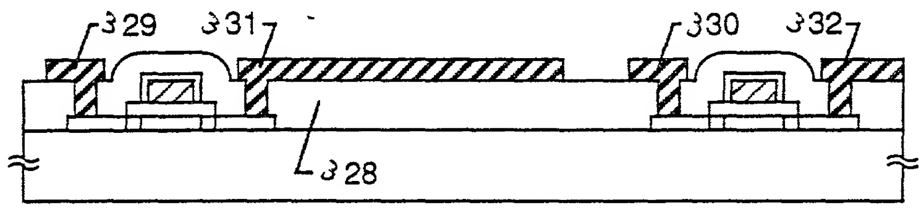

FIG. 4C

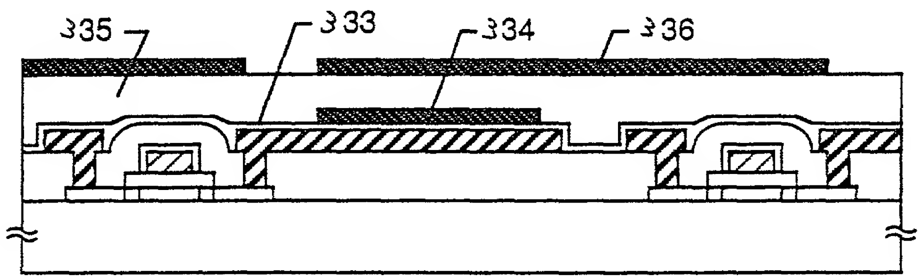

FIG. 4D

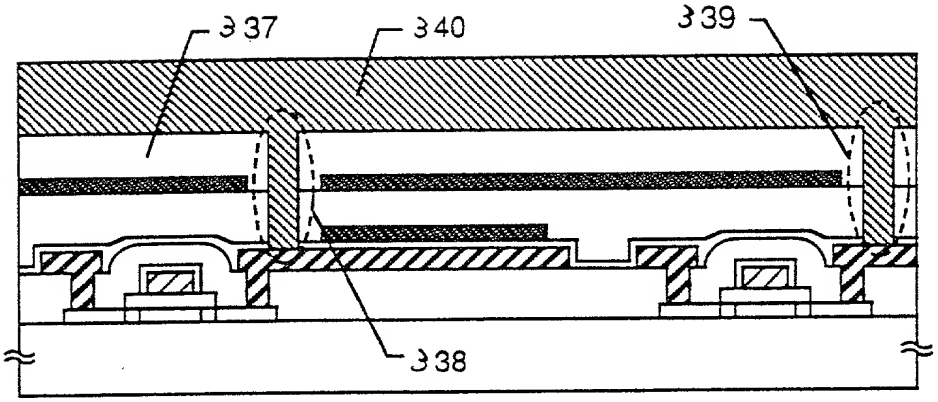

FIG. 5A

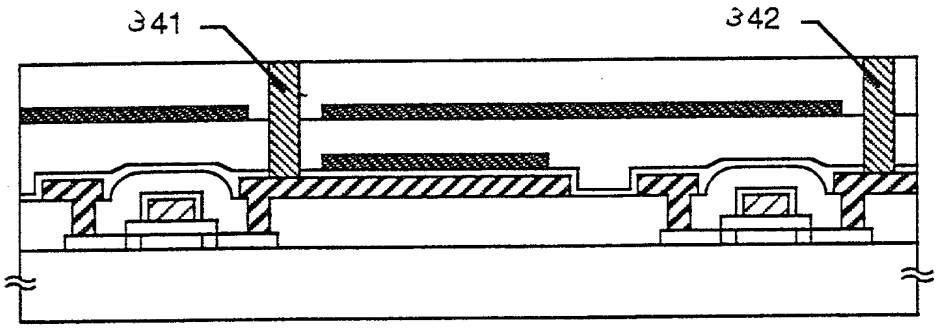

FIG. 5B

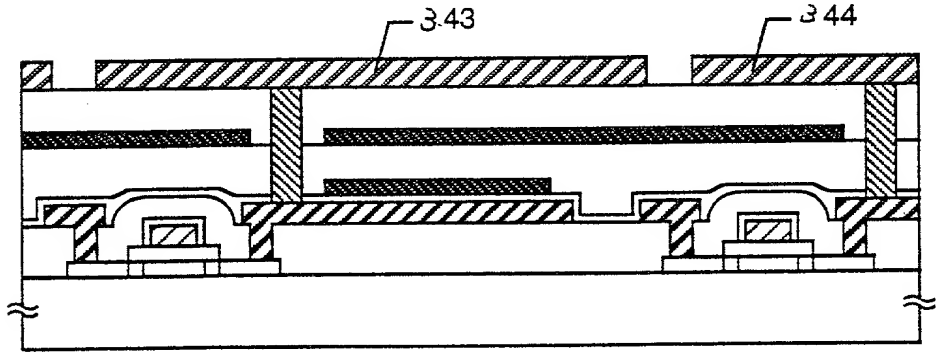

FIG. 5C

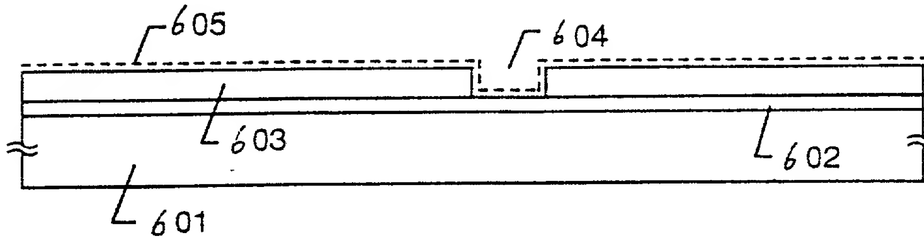

FIG. 6A

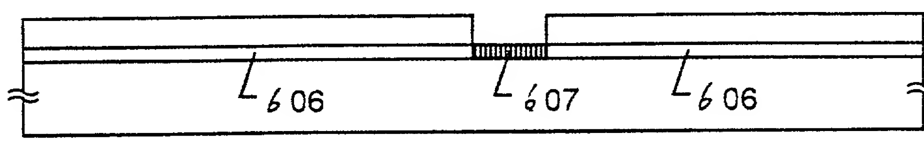

FIG. 6B

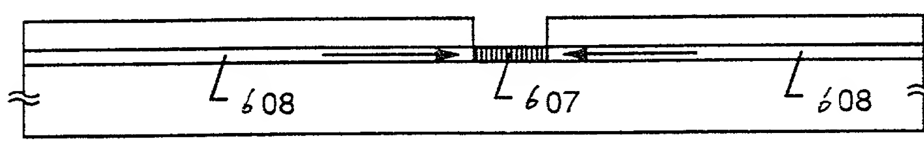

FIG. 6C

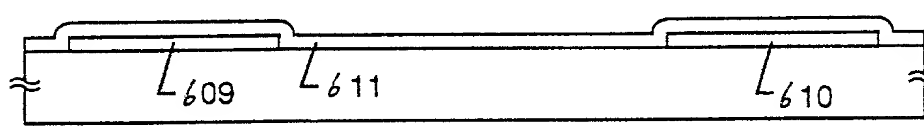

FIG. 6D

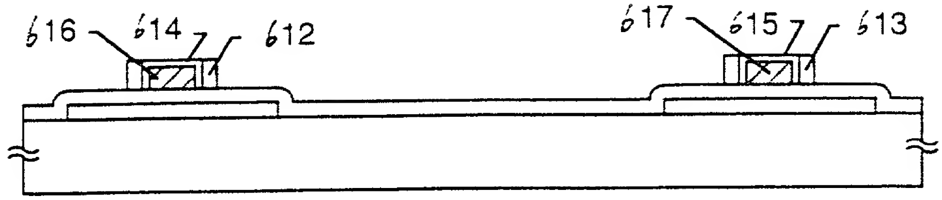

FIG. 7A

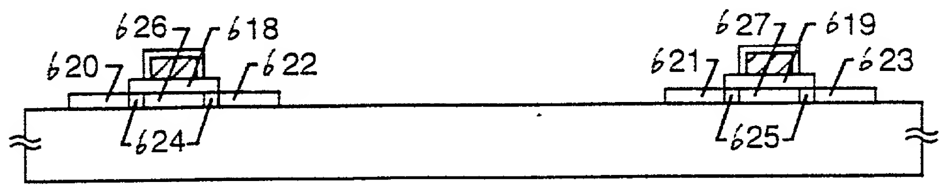

FIG. 7B

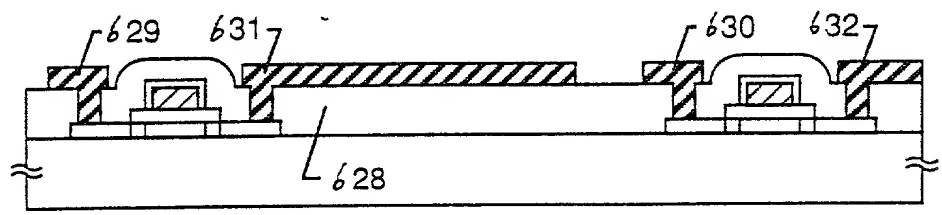

FIG. 7C

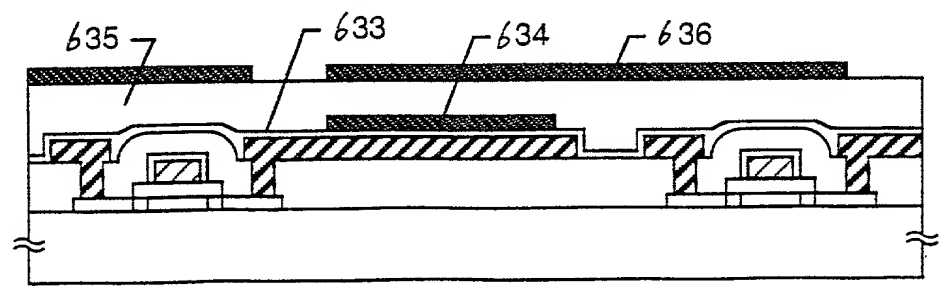

FIG. 7D

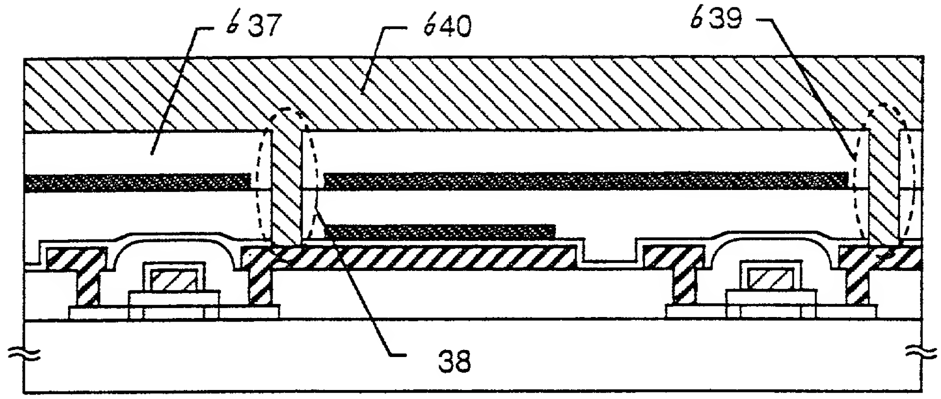

FIG. 8A

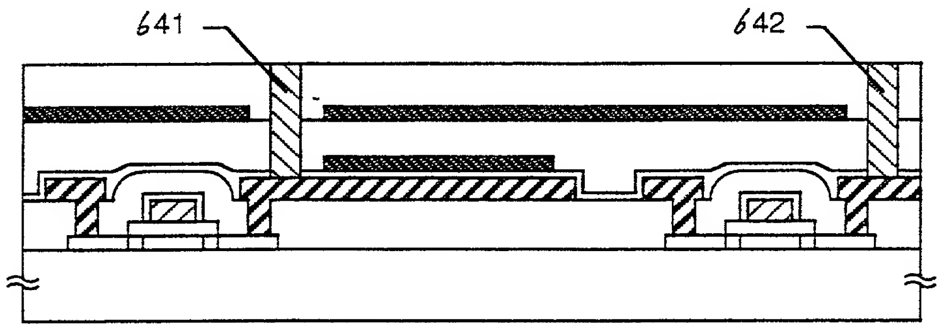

FIG. 8B

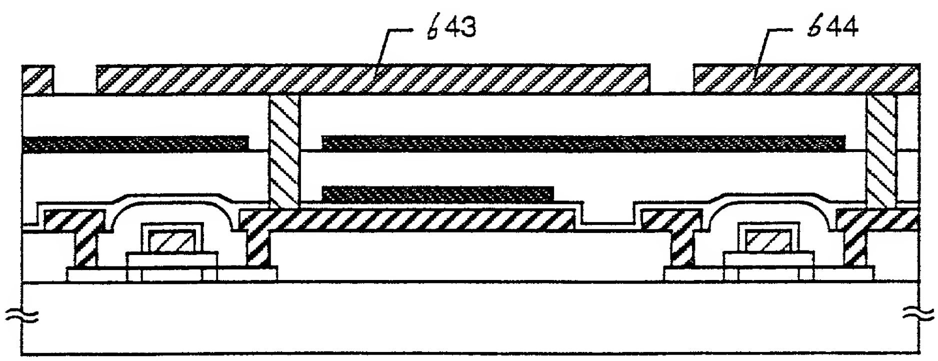

FIG. 8C

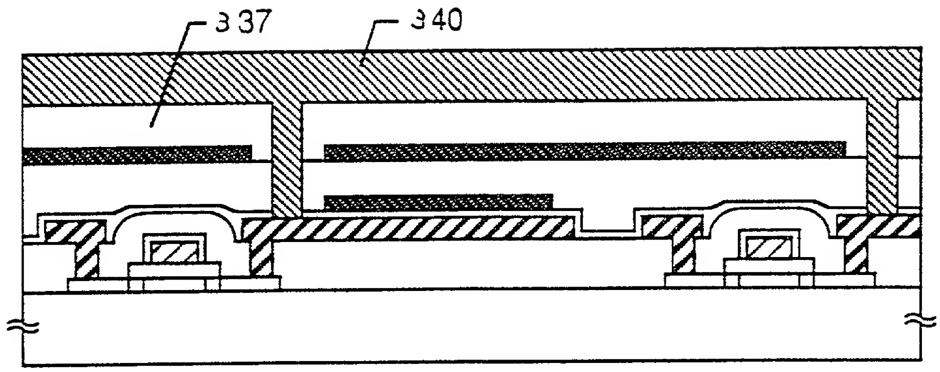

FIG. 9A

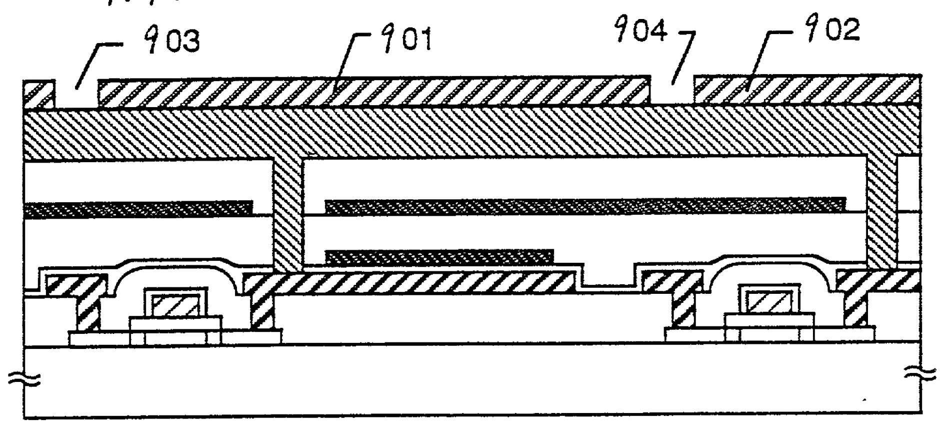

FIG. 9B

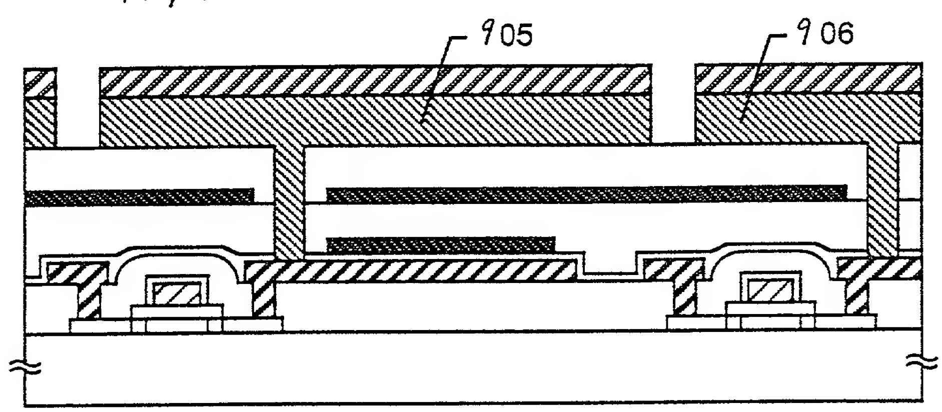

FIG. 9C

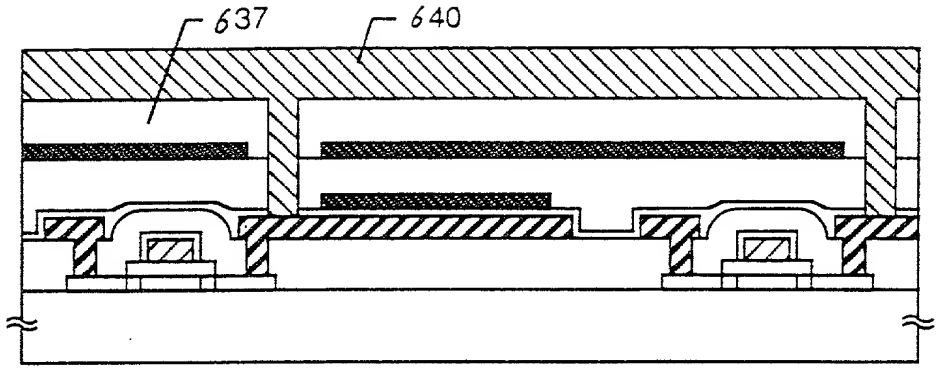

FIG. 10A

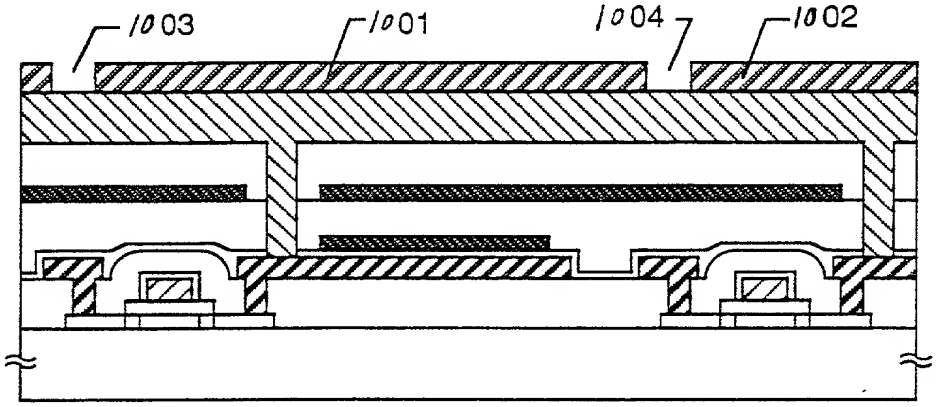

FIG. 10B

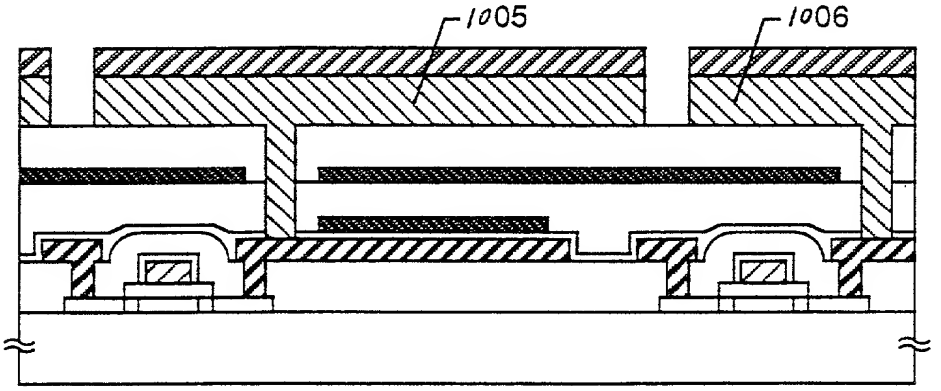

FIG. 10C

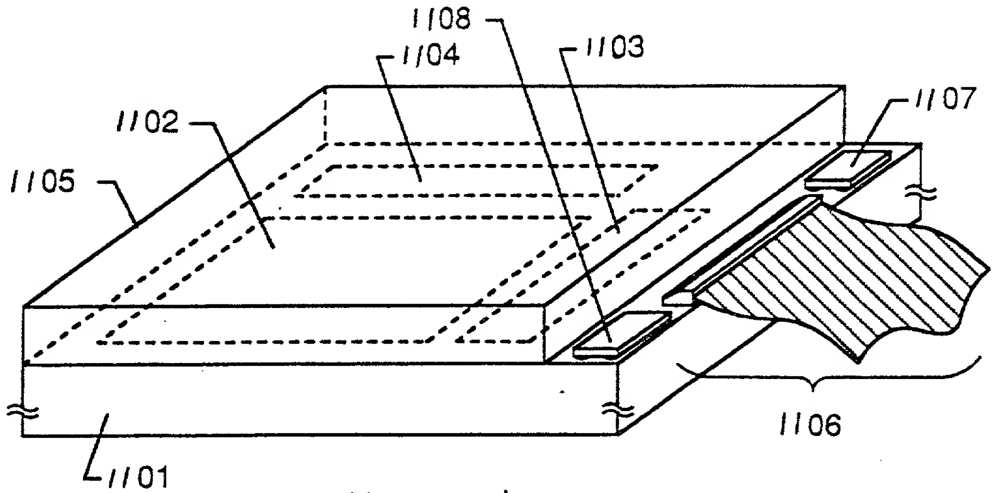

FIG. 11 A

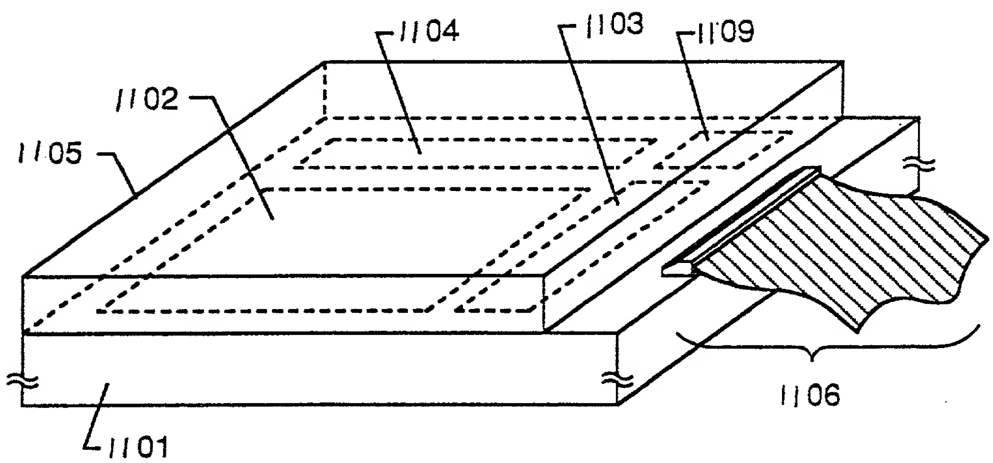

FIG. 11 B

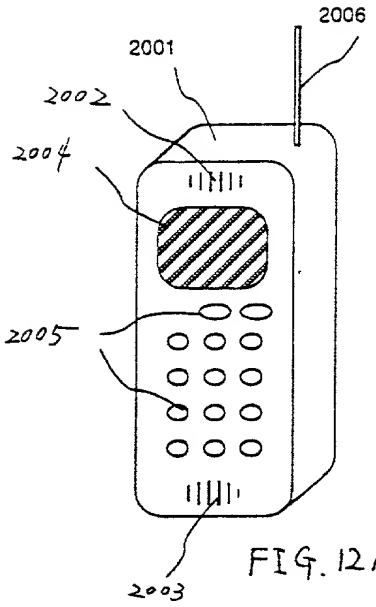

FIG. 12A

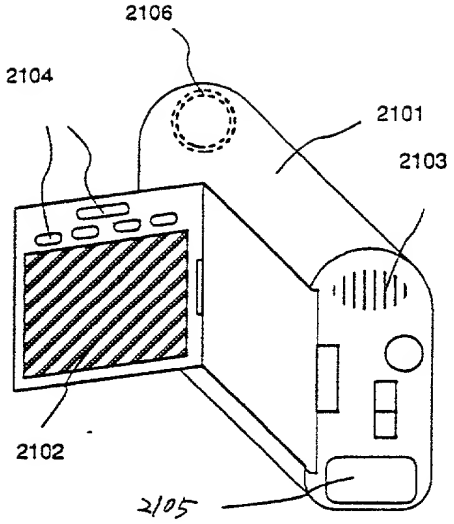

FIG. 12B

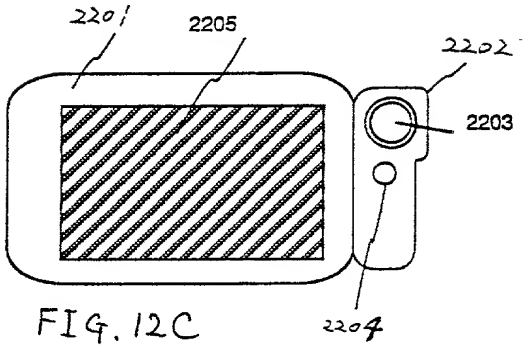

FIG. 12C

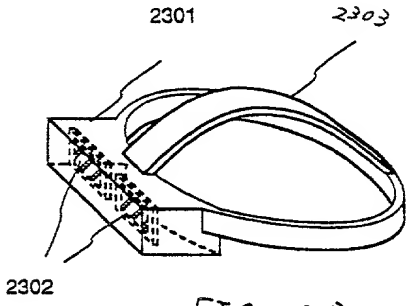

FIG. 12D

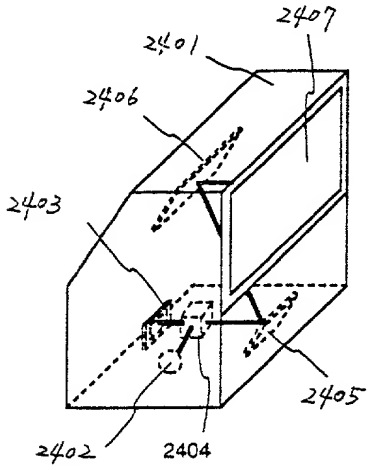

FIG. 12E

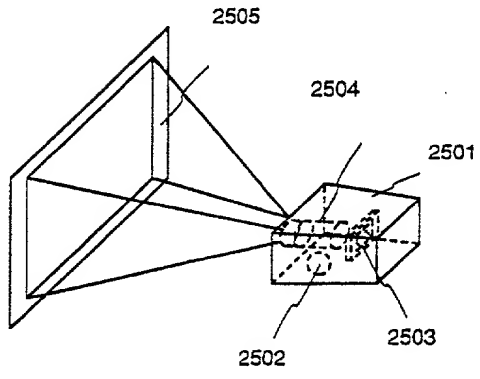

FIG. 12F

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

____

____

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR DEVICE AND PROCESS

FOR PRODUCING THE SAME

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を__________とし、（該当する場合）__________に訂正されました。

☐ was filed on ________________
as United States Application Number or
PCT International Application Number
__________ and was amended on
__________ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第 37 編第 1 条 56 項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration

(日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基き下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約365(a)項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			**Priority Not Claimed** 優先権主張なし
9-344350 (Number) (番号)	Japan (Country) (国名)	November 27, 1997 (Day/Month/Year Filed) (出願年月日)	☐
10-18050 (Number) (番号)	Japan (Country) (国名)	January 14, 1998 (Day/Month/Year Filed) (出願年月日)	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐

私は、第35編米国法典119条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第35編120条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条(c)に基く権利をここに主張します。また、本出願の各請求範囲の内容が米国法典代35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規制法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況・特許許可済、継続中、放棄済)

09550568.041700

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況: 特許許可済、継続中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況: 特許許可済、継続中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況: 特許許可済、継続中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況: 特許許可済、継続中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況: 特許許可済、継続中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況: 特許許可済、継続中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況: 特許許可済、継続中、放棄済)

私は、私自身の知識に基いて本宣言書中で私が行う表明が真実であり、かつ私の入手した情報と私の信じるところに基く表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第 18 編第 1001 条に基き、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行えば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状: 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁護士または代理人として、下記の者を指名いたします。(弁護士、または代理人の氏名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number).

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Eric J. Robinson (Reg. No. 38,285)
Joseph S. Presta (Reg. No. 35,329)
Thomas M. Blasey (Reg. No. 33,475)
Daniel S. Song (Reg. No. 43,143)

ここに署名する者は、この申請に関して米国特許商標局においてなされるべき如何なる行動に関しても、ここに指名された米国弁護士または代理人が、米国弁護士または代理人とここに署名した者との間で直接の連絡を取ることなしに、_____からの指示を受け入れてそれに従う権限を与える。指示を出す人物に変更がある場合は、ここに指名された米国弁護士または代理人は、ここに署名した者からその旨通知を受ける。

The undersigned hereby authorizes any U. S. attorney or agent named herein to accept and follow instructions from _____ as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U. S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U. S. attorneys or agents named herein will be so notified by the undersigned.

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Direct Telephone Calls to: (name and telephone number)

Gerald J. Ferguson, Jr.
(703) 790-9110

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		398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan	

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		Japanese
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		398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan

第三共同発明者		Full name of third joint inventor, if any
		Satoshi MURAKAMI
発明者の署名	日付	Inventor's signature Date
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国籍		Citizenship
		Japanese
私書箱		Post Office Address
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		398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan

第四共同発明者		Full name of fourth joint inventor, if any
発明者の署名	日付	Inventor's signature Date
住所		Residence
国籍		Citizenship
私書箱		Post Office Address

Docket No. 0756-2119

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Application of	)
Hisashi OHTANI et al.	)
Based On Serial No. 09/197,767	) Art Unit: 2814
Which Was Filed: November 23, 1998	) Examiner: P. Cao
For: SEMICONDUCTOR DEVICE AND	)
PROCESS FOR PRODUCING THE	)
SAME	) Date: April 17, 2000

NOTICE OF CHANGE OF COMPANY NAME

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231
Sir:

Effective immediately, please note that the company name of the attorney(s) of record in the above-referenced application has been changed. Please direct all future correspondence to:

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Respectfully submitted,

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